

CLAIMS

I Claim:

1 1. A three-dimensional stacked semiconductor package device, comprising:
2 a first semiconductor package device, comprising:
3 a first insulative housing with a first top surface, a first bottom surface, and a first
4 peripheral side surface between the first top and bottom surfaces;
5 a first semiconductor chip within the first insulative housing, wherein the first
6 chip includes a first upper surface and a first lower surface, and the first upper surface includes a
7 first conductive pad; and
8 a first lead that protrudes laterally from and extends through the first peripheral
9 side surface and is electrically connected to the first pad, wherein the first lead outside the first
10 insulative housing is bent downwardly;
11 a second semiconductor package device, comprising:
12 a second insulative housing with a second top surface, a second bottom surface,
13 and a second peripheral side surface between the second top and bottom surfaces;
14 a second semiconductor chip within the second insulative housing, wherein the
15 second chip includes a second upper surface and a second lower surface, and the second upper
16 surface includes a second conductive pad; and
17 a second lead that protrudes laterally from and extends through the second
18 peripheral side surface and is electrically connected to the second pad, wherein the second lead
19 outside the second insulative housing is flat; and
20 a conductive bond outside the insulative housings that extends laterally beyond any
21 insulative material of the stacked device, extends downwardly beyond a surface of the first chip
22 and contacts and electrically connects the leads;
23 wherein the second insulative housing overlaps the first insulative housing, the second
24 lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the
25 bottom surfaces face downwardly, and the first top surface faces towards the second bottom
26 surface.

1 2. The stacked device of claim 1, wherein the first upper surface faces towards the
2 first bottom surface, and the second upper surface faces towards the second bottom surface.

1 3. The stacked device of claim 1, wherein the first lead extends downwardly beyond
2 the first bottom surface outside the first insulative housing, and the second lead does not extend
3 downwardly beyond the second bottom surface outside the second insulative housing.

1 4. The stacked device of claim 1, wherein the first lead extends laterally from the
2 first peripheral side surface a first distance, the second lead extends laterally from the second
3 peripheral side surface a second distance, and the first distance is greater than the second
4 distance.

1 5. The stacked device of claim 1, wherein the first lead outside the first insulative
2 housing includes inner and outer corners that are bent, an inner lateral portion that extends
3 laterally between the first peripheral side surface and the inner corner, a sloped portion that
4 extends laterally and downwardly between the inner and outer corners, and an outer lateral
5 portion that extends laterally between the outer corner and a distal end.

1 6. The stacked device of claim 5, wherein the second lead outside the second
2 insulative housing is essentially identical to the inner lateral portion of the first lead.

1 7. The stacked device of claim 1, wherein the conductive bond is spaced from the
2 insulative housings.

1 8. The stacked device of claim 1, wherein the conductive bond is outside the
2 peripheries of the insulative housings.

1 9. The stacked device of claim 1, wherein the conductive bond has a substantially
2 spherical shape.

1 10. The stacked device of claim 1, wherein the stacked device is devoid of wire bonds
2 and TAB leads.

1 11. A three-dimensional stacked semiconductor package device, comprising:
2 a first semiconductor package device, comprising:
3 a first insulative housing with a first top surface, a first bottom surface, and a first
4 peripheral side surface between the first top and bottom surfaces;
5 a first semiconductor chip within the first insulative housing, wherein the first
6 chip includes a first upper surface and a first lower surface, and the first upper surface includes a
7 first conductive pad; and
8 a first lead that protrudes laterally from and extends through the first peripheral
9 side surface and is electrically connected to the first pad, wherein the first lead outside the first
10 insulative housing is bent downwardly, extends laterally from the first peripheral side surface a
11 first distance, and extends downwardly beyond the first bottom surface;
12 a second semiconductor package device, comprising:
13 a second insulative housing with a second top surface, a second bottom surface,
14 and a second peripheral side surface between the second top and bottom surfaces;
15 a second semiconductor chip within the second insulative housing, wherein the
16 second chip includes a second upper surface and a second lower surface, and the second upper
17 surface includes a second conductive pad; and
18 a second lead that protrudes laterally from and extends through the second
19 peripheral side surface and is electrically connected to the second pad, wherein the second lead
20 outside the second insulative housing is flat, extends laterally from the second peripheral side
21 surface a second distance, and does not extend downwardly beyond the second bottom surface;
22 and
23 a conductive bond outside the insulative housings that extends laterally beyond any
24 insulative material of the stacked device, extends downwardly beyond a surface of the first chip
25 and contacts and electrically connects the leads;
26 wherein the second insulative housing overlaps the first insulative housing, the second
27 lead overlaps the first lead outside the insulative housings, the leads do not contact any insulative

28 material of the stacked device outside the insulative housings, the top surfaces face upwardly, the
29 bottom surfaces face downwardly, the first top surface faces towards the second bottom surface,
30 and the first distance is greater than the second distance.

1 12. The stacked device of claim 11, wherein the first upper surface faces towards the
2 first bottom surface, and the second upper surface faces towards the second bottom surface.

1 13. The stacked device of claim 11, wherein the insulative housings are essentially
2 identical to and vertically aligned with one another.

1 14. The stacked device of claim 11, wherein the first lead is adjacent to the first
2 bottom surface, and the second lead is adjacent to the second bottom surface.

1 15. The stacked device of claim 11, wherein the first lead includes inner and outer
2 corners that are bent, an inner lateral portion that extends laterally between the first peripheral
3 side surface and the inner corner, a sloped portion that extends laterally and downwardly between
4 the inner and outer corners, and an outer lateral portion that extends laterally between the outer
5 corner and a distal end.

1 16. The stacked device of claim 15, wherein the second lead outside the second
2 insulative housing is essentially identical to the inner lateral portion of the first lead.

1 17. The stacked device of claim 11, wherein the conductive bond is spaced from the
2 insulative housings and outside the peripheries of the insulative housings.

1 18. The stacked device of claim 11, wherein the conductive bond contacts only the
2 leads.

1 19. The stacked device of claim 11, wherein the conductive bond has a substantially
2 spherical shape.

1 20. The stacked device of claim 11, wherein the stacked device is devoid of wire
2 bonds and TAB leads.

1 21. A three-dimensional stacked semiconductor package device, comprising:
2 a first semiconductor package device, comprising:
3 a first insulative housing with a first top surface, a first bottom surface, and a first
4 peripheral side surface between the first top and bottom surfaces, wherein the first bottom surface
5 includes a first peripheral ledge and a first central portion that is within and recessed relative to
6 and non-integral with the first peripheral ledge;
7 a first semiconductor chip within the first insulative housing, wherein the first
8 chip includes a first upper surface and a first lower surface, and the first upper surface includes a
9 first conductive pad; and
10 a first lead that protrudes laterally from and extends through the first peripheral
11 side surface and is electrically connected to the first pad, wherein the first lead outside the first
12 insulative housing is bent downwardly, extends laterally from the first peripheral side surface at
13 the first peripheral ledge, and extends downwardly beyond the first bottom surface at the first
14 peripheral ledge;
15 a second semiconductor package device, comprising:
16 a second insulative housing with a second top surface, a second bottom surface,
17 and a second peripheral side surface between the second top and bottom surfaces, wherein the
18 second bottom surface includes a second peripheral ledge and a second central portion that is
19 within and recessed relative to and non-integral with the second peripheral ledge;
20 a second semiconductor chip within the second insulative housing, wherein the
21 second chip includes a second upper surface and a second lower surface, and the second upper
22 surface includes a second conductive pad; and
23 a second lead that protrudes laterally from and extends through the second
24 peripheral side surface and is electrically connected to the second pad, wherein the second lead
25 outside the second insulative housing is flat, extends laterally from the second peripheral side

26 surface at the second peripheral ledge, and does not extend downwardly beyond the second
27 bottom surface at the second peripheral ledge; and
28 a conductive bond outside the insulative housings that extends laterally beyond any
29 insulative material of the stacked device and contacts and electrically connects the leads;
30 wherein the insulative housings are essentially identical to and vertically aligned with one
31 another, the second insulative housing overlaps the first insulative housing, the second lead
32 overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom
33 surfaces face downwardly, and the first top surface faces towards the second bottom surface.

1 22. The stacked device of claim 21, wherein the first upper surface faces towards the
2 first bottom surface, and the second upper surface faces towards the second bottom surface.

1 23. The stacked device of claim 21, wherein the first lead extends laterally from the
2 first peripheral side surface a first distance, the second lead extends laterally from the second
3 peripheral side surface a second distance, and the first distance is greater than the second
4 distance.

1 24. The stacked device of claim 21, wherein the first lead is adjacent to the first
2 bottom surface, and the second lead is adjacent to the second bottom surface.

1 25. The stacked device of claim 21, wherein the first lead includes inner and outer
2 corners that are bent, an inner lateral portion that extends laterally between the first peripheral
3 side surface and the inner corner, a sloped portion that extends laterally and downwardly between
4 the inner and outer corners, and an outer lateral portion that extends laterally between the outer
5 corner and a distal end.

1 26. The stacked device of claim 25, wherein the second lead outside the second
2 insulative housing is essentially identical to the inner lateral portion of the first lead.

1 27. The stacked device of claim 21, wherein the conductive bond is spaced from the
2 insulative housings and outside the peripheries of the insulative housings.

1 28. The stacked device of claim 21, wherein the conductive bond contacts only the
2 leads.

1 29. The stacked device of claim 21, wherein the conductive bond has a substantially
2 spherical shape.

1 30. The stacked device of claim 21, wherein the stacked device is devoid of wire
2 bonds and TAB leads.

1 31. A three-dimensional stacked semiconductor package device, comprising:
2 a first semiconductor package device, comprising:
3 a first insulative housing with a first top surface, a first bottom surface, and a first
4 peripheral side surface between the first top and bottom surfaces;
5 a first semiconductor chip within the first insulative housing, wherein the first
6 chip includes a first upper surface and a first lower surface, and the first upper surface includes a
7 first conductive pad; and
8 a first lead that protrudes laterally from and extends through the first peripheral
9 side surface and is electrically connected to the first pad, wherein the first lead outside the first
10 insulative housing includes inner and outer corners that are bent, an inner lateral portion that
11 extends laterally between the first peripheral side surface and the inner corner, a sloped portion
12 that extends laterally and downwardly between the inner and outer corners, and an outer lateral
13 portion that extends laterally between the outer corner and a first distal end;
14 a second semiconductor package device, comprising:
15 a second insulative housing with a second top surface, a second bottom surface,
16 and a second peripheral side surface between the second top and bottom surfaces;

17 a second semiconductor chip within the second insulative housing, wherein the
18 second chip includes a second upper surface and a second lower surface, and the second upper
19 surface includes a second conductive pad; and
20 a second lead that protrudes laterally from and extends through the second
21 peripheral side surface and is electrically connected to the second pad, wherein the second lead
22 outside the second insulative housing is flat and extends laterally between the second peripheral
23 side surface and a second distal end; and
24 a conductive bond outside the insulative housings and outside the peripheries of the
25 insulative housings that extends laterally beyond any insulative material of the stacked device,
26 contacts and electrically connects the leads and does not contact any other material;
27 wherein the insulative housings are essentially identical to and vertically aligned with one
28 another, the second insulative housing overlaps the first insulative housing, the second lead
29 overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom
30 surfaces face downwardly, and the first top surface faces towards the second bottom surface.

1 32. The stacked device of claim 31, wherein the first upper surface faces towards the
2 first bottom surface, and the second upper surface faces towards the second bottom surface.

1 33. The stacked device of claim 31, wherein the first lead is adjacent to the first
2 bottom surface, and the second lead is adjacent to the second bottom surface.

1 34. The stacked device of claim 31, wherein the second corner laterally extends a first
2 distance from the first peripheral side surface, the second distal end laterally extends a second
3 distance from the second peripheral side surface, and the first distance is greater than the second
4 distance.

1 35. The stacked device of claim 31, wherein the first corner laterally extends a first
2 distance from the first peripheral side surface, the second distal end laterally extends a second
3 distance from the second peripheral side surface, and the first and second distances are
4 essentially identical.

1 36. The stacked device of claim 31, wherein the conductive bond is laterally aligned
2 with the second bottom surface.

1 37. The stacked device of claim 31, wherein the conductive bond is closer to the
2 second bottom surface than to the first bottom surface.

1 38. The stacked device of claim 31, wherein the conductive bond contacts only the
2 inner lateral portion and the second lead.

1 39. The stacked device of claim 31, wherein the conductive bond has a substantially
2 spherical shape.

1 40. The stacked device of claim 31, wherein the stacked device is devoid of wire
2 bonds and TAB leads.

1 41. A three-dimensional stacked semiconductor package device, comprising:
2 a first semiconductor package device, comprising:
3 a first insulative housing with a first top surface, a first bottom surface, and a first
4 peripheral side surface between the first top and bottom surfaces;
5 a first semiconductor chip within the first insulative housing, wherein the first
6 chip includes a first upper surface and a first lower surface, and the first upper surface includes a
7 first conductive pad; and
8 a first lead that protrudes laterally from and extends through the first peripheral
9 side surface and is electrically connected to the first pad, wherein the first lead outside the first
10 insulative housing is bent downwardly and extends downwardly beyond the first bottom surface;
11 a second semiconductor package device, comprising:
12 a second insulative housing with a second top surface, a second bottom surface,
13 and a second peripheral side surface between the second top and bottom surfaces;

14 a second semiconductor chip within the second insulative housing, wherein the
15 second chip includes a second upper surface and a second lower surface, and the second upper
16 surface includes a second conductive pad; and
17 a second lead that protrudes laterally from and extends through the second
18 peripheral side surface and is electrically connected to the second pad, wherein the second lead
19 outside the second insulative housing is flat; and
20 a conductive bond outside the insulative housings that extends laterally beyond any
21 insulative material of the stacked device, does not overlap any insulative material of the stacked
22 device, is not overlapped by any insulative material of the stacked device and contacts and
23 electrically connects the leads;
24 wherein the second insulative housing overlaps the first insulative housing, the second
25 lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the
26 bottom surfaces face downwardly, and the first top surface faces towards the second bottom
27 surface.

1 42. The stacked device of claim 41, wherein the first upper surface faces towards the
2 first bottom surface, and the second upper surface faces towards the second bottom surface.

1 43. The stacked device of claim 41, wherein the first lead is adjacent to the first
2 bottom surface, and the second lead is adjacent to the second bottom surface.

1 44. The stacked device of claim 41, wherein the first lead includes inner and outer
2 corners that are bent, an inner lateral portion that extends laterally between the first peripheral
3 side surface and the inner corner, a sloped portion that extends laterally and downwardly between
4 the inner and outer corners, and an outer lateral portion that extends laterally between the outer
5 corner and a distal end.

1 45. The stacked device of claim 44, wherein the second lead outside the second
2 insulative housing is essentially identical to the inner lateral portion of the first lead.

1 46. The stacked device of claim 41, wherein the conductive bond is laterally aligned
2 with the second bottom surface, and is not laterally aligned with the first bottom surface.

1 47. The stacked device of claim 41, wherein the conductive bond does not contact any
2 insulative material of the stacked device.

1 48. The stacked device of claim 41, wherein the conductive bond contacts only the
2 leads.

1 49. The stacked device of claim 41, wherein the conductive bond has a substantially
2 spherical shape.

1 50. The stacked device of claim 41, wherein the stacked device is devoid of wire
2 bonds and TAB leads.

1 51. A three-dimensional stacked semiconductor package device, comprising:
2 a first semiconductor package device, comprising:
3 a first insulative housing with a first top surface, a first bottom surface, and a first
4 peripheral side surface between the first top and bottom surfaces;
5 a first semiconductor chip within the first insulative housing, wherein the first
6 chip includes a first upper surface and a first lower surface, and the first upper surface includes a
7 first conductive pad; and
8 a first lead that protrudes laterally from and extends through the first peripheral
9 side surface and is electrically connected to the first pad, wherein the first lead outside the first
10 insulative housing is bent downwardly, extends laterally from the first peripheral side surface a
11 first distance, extends downwardly beyond the first bottom surface, does not overlap any
12 insulative material of the first device and is not overlapped by any insulative material of the first
13 device;
14 a second semiconductor package device, comprising:

15 a second insulative housing with a second top surface, a second bottom surface,
16 and a second peripheral side surface between the second top and bottom surfaces;

17 a second semiconductor chip within the second insulative housing, wherein the
18 second chip includes a second upper surface and a second lower surface, and the second upper
19 surface includes a second conductive pad; and

20 a second lead that protrudes laterally from and extends through the second
21 peripheral side surface and is electrically connected to the second pad, wherein the second lead
22 outside the second insulative housing is flat, extends laterally from the second peripheral side
23 surface a second distance, does not extend downwardly beyond the second bottom surface, does
24 not overlap any insulative material of the second device and is not overlapped by any insulative
25 material of the second device; and

26 a conductive bond outside the insulative housings that extends laterally beyond any
27 insulative material of the stacked device, does not overlap any insulative material of the stacked
28 device, is not overlapped by any insulative material of the stacked device, extends laterally
29 beyond the first peripheral side surface a third distance and contacts and electrically connects the
30 leads;

31 wherein the insulative housings are essentially identical to and vertically aligned with one
32 another, the second insulative housing overlaps the first insulative housing, the second lead
33 overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom
34 surfaces face downwardly, the first top surface faces towards the second bottom surface, and the
35 first distance is greater than the second and third distances.

1 52. The stacked device of claim 51, wherein the first upper surface faces towards the
2 first bottom surface, and the second upper surface faces towards the second bottom surface.

1 53. The stacked device of claim 51, wherein the first lead is adjacent to the first
2 bottom surface, and the second lead is adjacent to the second bottom surface.

1 54. The stacked device of claim 51, wherein the first lead includes inner and outer
2 corners that are bent, an inner lateral portion that extends laterally between the first peripheral

3 side surface and the inner corner, a sloped portion that extends laterally and downwardly between
4 the inner and outer corners, and an outer lateral portion that extends laterally between the outer
5 corner and a distal end.

1 55. The stacked device of claim 54, wherein the second lead outside the second
2 insulative housing is essentially identical to the inner lateral portion of the first lead.

1 56. The stacked device of claim 51, wherein the conductive bond is laterally aligned
2 with the second bottom surface, and is not laterally aligned with the first bottom surface.

1 57. The stacked device of claim 51, wherein the conductive bond does not contact any
2 insulative material of the stacked device.

1 58. The stacked device of claim 51, wherein the conductive bond contacts only the
2 leads.

1 59. The stacked device of claim 51, wherein the conductive bond has a substantially
2 spherical shape.

1 60. The stacked device of claim 51, wherein the stacked device is devoid of wire
2 bonds and TAB leads.

1 61. A three-dimensional stacked semiconductor package device, comprising:
2 a first semiconductor package device, comprising:
3 a first insulative housing with a first top surface, a first bottom surface, and a first
4 peripheral side surface between the first top and bottom surfaces;
5 a first semiconductor chip within the first insulative housing, wherein the first
6 chip includes a first upper surface and a first lower surface, and the first upper surface includes a
7 first conductive pad; and

8 a first lead that protrudes laterally from and extends through the first peripheral
9 side surface and is electrically connected to the first pad, wherein the first lead outside the first
10 insulative housing is bent downwardly;

11 a second semiconductor package device, comprising:

12 a second insulative housing with a second top surface, a second bottom surface,
13 and a second peripheral side surface between the second top and bottom surfaces;

14 a second semiconductor chip within the second insulative housing, wherein the
15 second chip includes a second upper surface and a second lower surface, and the second upper
16 surface includes a second conductive pad; and

17 a second lead that protrudes laterally from and extends through the second
18 peripheral side surface and is electrically connected to the second pad, wherein the second lead
19 outside the second insulative housing is flat;

20 a third semiconductor package device, comprising:

21 a third insulative housing with a third top surface, a third bottom surface, and a
22 third peripheral side surface between the third top and bottom surfaces;

23 a third semiconductor chip within the third insulative housing, wherein the third
24 chip includes a third upper surface and a third lower surface, and the third upper surface includes
25 a third conductive pad; and

26 a third lead that protrudes laterally from and extends through the third peripheral
27 side surface and is electrically connected to the third pad, wherein the third lead outside the third
28 insulative housing is flat;

29 a first conductive bond outside the insulative housings that extends laterally beyond any
30 insulative material of the stacked device and contacts and electrically connects the first and
31 second leads; and

32 a second conductive bond outside the insulative housings that extends laterally beyond
33 any insulative material of the stacked device and contacts and electrically connects the second
34 and third leads;

35 wherein the third insulative housing overlaps the second insulative housing, the second
36 insulative housing overlaps the first insulative housing, the third lead overlaps the second lead
37 outside the insulative housings, the second lead overlaps the first lead outside the insulative

38 housings, the top surfaces face upwardly, the bottom surfaces face downwardly, the first top
39 surface faces towards the second bottom surface, and the second top surface faces towards the
40 third bottom surface.

1 62. The stacked device of claim 61, wherein the first upper surface faces towards the
2 first bottom surface, the second upper surface faces towards the second bottom surface, and the
3 third upper surface faces towards the third bottom surface.

1 63. The stacked device of claim 61, wherein the first lead extends downwardly
2 beyond the first bottom surface outside the first insulative housing, the second lead does not
3 extend downwardly beyond the second bottom surface outside the second insulative housing, and
4 the third lead does not extend downwardly beyond the third bottom surface outside the third
5 insulative housing.

1 64. The stacked device of claim 61, wherein the first lead extends laterally from the
2 first peripheral side surface a first distance, the second lead extends laterally from the second
3 peripheral side surface a second distance, the third lead extends laterally from the third peripheral
4 side surface a third distance, and the first distance is greater than the second and third distances.

1 65. The stacked device of claim 61, wherein the first lead outside the first insulative
2 housing includes inner and outer corners that are bent, an inner lateral portion that extends
3 laterally between the first peripheral side surface and the inner corner, a sloped portion that
4 extends laterally and downwardly between the inner and outer corners, and an outer lateral
5 portion that extends laterally between the outer corner and a distal end.

1 66. The stacked device of claim 65, wherein the second lead outside the second
2 insulative housing and the third lead outside the third insulative housing are essentially identical
3 to the inner lateral portion of the first lead.

1 67. The stacked device of claim 61, wherein the conductive bonds are spaced from the
2 insulative housings.

1 68. The stacked device of claim 61, wherein the conductive bonds are outside the
2 peripheries of the insulative housings.

1 69. The stacked device of claim 61, wherein the conductive bonds have substantially
2 spherical shapes.

1 70. The stacked device of claim 61, wherein the stacked device is devoid of wire
2 bonds and TAB leads.

1 71. A three-dimensional stacked semiconductor package device, comprising:
2 a first semiconductor package device, comprising:
3 a first insulative housing with a first top surface, a first bottom surface, and a first
4 peripheral side surface between the first top and bottom surfaces, wherein the first bottom surface
5 includes a peripheral ledge and a central portion that is within and recessed relative to the
6 peripheral ledge, and the peripheral ledge and the central portion form a cavity;
7 a first semiconductor chip within the first insulative housing, wherein the first
8 chip includes a first upper surface and a first lower surface, and the first upper surface includes a
9 first conductive pad;
10 a first lead that protrudes laterally from and extends through the first peripheral
11 side surface and is electrically connected to the first pad, wherein the first lead outside the first
12 insulative housing is bent downwardly; and
13 a first terminal that extends through the central portion, is spaced from the first
14 peripheral side surface, is spaced and separated from the first lead outside the first insulative
15 housing and is electrically connected to the first lead and the first pad inside the first insulative
16 housing; and
17 a second semiconductor package device, comprising:

18 a second insulative housing with a second top surface, a second bottom surface,
19 and a second peripheral side surface between the second top and bottom surfaces;
20 a second semiconductor chip within the second insulative housing, wherein the
21 second chip includes a second upper surface and a second lower surface, and the second upper
22 surface includes a second conductive pad; and
23 a second lead that protrudes laterally from and extends through the second
24 peripheral side surface and is electrically connected to the second pad, wherein the second lead
25 outside the second insulative housing is flat;
26 a third semiconductor package device, comprising:
27 a third insulative housing;
28 a third semiconductor chip within the third insulative housing, wherein the third
29 chip includes a third upper surface and a third lower surface, and the third upper surface includes
30 a third conductive pad; and
31 a third terminal that extends through the third insulative housing and is
32 electrically connected to the third pad;
33 a first conductive bond outside the insulative housings that extends laterally beyond any
34 insulative material of the stacked device and contacts and electrically connects the leads; and
35 a second conductive bond inside the cavity that contacts and electrically connects the
36 terminals;
37 wherein the second insulative housing overlaps the first insulative housing, the second
38 lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the
39 bottom surfaces face downwardly, the first top surface faces towards the second bottom surface,
40 the first terminal overlaps the third terminal, and the third device extends into the cavity and does
41 not extend outside a periphery of the cavity.

1 72. The stacked device of claim 71, wherein the first upper surface faces towards the
2 first bottom surface, and the second upper surface faces towards the second bottom surface.

1 73. The stacked device of claim 71, wherein the first lead extends downwardly
2 beyond the first bottom surface outside the first insulative housing, and the second lead does not
3 extend downwardly beyond the second bottom surface outside the second insulative housing.

1 74. The stacked device of claim 71, wherein the first lead extends laterally from the
2 first peripheral side surface a first distance, the second lead extends laterally from the second
3 peripheral side surface a second distance, and the first distance is greater than the second
4 distance.

1 75. The stacked device of claim 71, wherein the first lead outside the first insulative
2 housing includes inner and outer corners that are bent, an inner lateral portion that extends
3 laterally between the first peripheral side surface and the inner corner, a sloped portion that
4 extends laterally and downwardly between the inner and outer corners, and an outer lateral
5 portion that extends laterally between the outer corner and a distal end.

1 76. The stacked device of claim 75, wherein the second lead outside the second
2 insulative housing is essentially identical to the inner lateral portion of the first lead.

1 77. The stacked device of claim 71, wherein the first conductive bond is spaced from
2 the insulative housings.

1 78. The stacked device of claim 71, wherein the first conductive bond is outside the
2 peripheries of the insulative housings.

1 79. The stacked device of claim 71, wherein the first conductive bond has a
2 substantially spherical shape.

1 80. The stacked device of claim 71, wherein the stacked device is devoid of wire
2 bonds and TAB leads.

1 81. A three-dimensional stacked semiconductor package device, comprising:

2 a first semiconductor package device, comprising:

3 a first insulative housing with a first top surface, a first bottom surface, and a first
4 peripheral side surface between the first top and bottom surfaces;

5 a first semiconductor chip within the first insulative housing, wherein the first
6 chip includes a first upper surface and a first lower surface, and the first upper surface includes a
7 first conductive pad; and

8 a first lead that protrudes laterally from and extends through the first peripheral
9 side surface and is electrically connected to the first pad, wherein the first lead outside the first
10 insulative housing is bent downwardly;

11 a second semiconductor package device, comprising:

12 a second insulative housing with a second top surface, a second bottom surface,
13 and a second peripheral side surface between the second top and bottom surfaces, wherein the
14 second bottom surface includes a peripheral ledge and a central portion that is within and
15 recessed relative to the peripheral ledge, and the peripheral ledge and the central portion form a
16 cavity;

17 a second semiconductor chip within the second insulative housing, wherein the
18 second chip includes a second upper surface and a second lower surface, and the second upper
19 surface includes a second conductive pad;

20 a second lead that protrudes laterally from and extends through the second
21 peripheral side surface and is electrically connected to the second pad, wherein the second lead
22 outside the second insulative housing is flat; and

23 a second terminal that extends through the central portion, is spaced from the
24 second peripheral side surface, is spaced and separated from the second lead outside the second
25 insulative housing and is electrically connected to the second lead and the second pad inside the
26 second insulative housing;

27 a third semiconductor package device, comprising:

28 a third insulative housing;

29 a third semiconductor chip within the third insulative housing, wherein the third
30 chip includes a third upper surface and a third lower surface, and the third upper surface includes
31 a third conductive pad; and
32 a third terminal that extends through the third insulative housing and is
33 electrically connected to the third pad;
34 a first conductive bond outside the insulative housings that extends laterally beyond any
35 insulative material of the stacked device and contacts and electrically connects the leads; and
36 a second conductive bond inside the cavity that contacts and electrically connects the
37 terminals;
38 wherein the second insulative housing overlaps the first insulative housing, the second
39 lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the
40 bottom surfaces face downwardly, the first top surface faces towards the second bottom surface,
41 the second terminal overlaps the third terminal, and the third device extends into the cavity and
42 does not extend outside a periphery of the cavity.

1 82. The stacked device of claim 81, wherein the first upper surface faces towards the
2 first bottom surface, and the second upper surface faces towards the second bottom surface.

1 83. The stacked device of claim 81, wherein the first lead extends downwardly
2 beyond the first bottom surface outside the first insulative housing, and the second lead does not
3 extend downwardly beyond the second bottom surface outside the second insulative housing.

1 84. The stacked device of claim 81, wherein the first lead extends laterally from the
2 first peripheral side surface a first distance, the second lead extends laterally from the second
3 peripheral side surface a second distance, and the first distance is greater than the second
4 distance.

1 85. The stacked device of claim 81, wherein the first lead outside the first insulative
2 housing includes inner and outer corners that are bent, an inner lateral portion that extends
3 laterally between the first peripheral side surface and the inner corner, a sloped portion that

4 extends laterally and downwardly between the inner and outer corners, and an outer lateral
5 portion that extends laterally between the outer corner and a distal end.

1 86. The stacked device of claim 85, wherein the second lead outside the second
2 insulative housing is essentially identical to the inner lateral portion of the first lead.

1 87. The stacked device of claim 81, wherein the first conductive bond is spaced from
2 the insulative housings.

1 88. The stacked device of claim 81, wherein the first conductive bond is outside the
2 peripheries of the insulative housings.

1 89. The stacked device of claim 81, wherein the first conductive bond has a
2 substantially spherical shape.

1 90. The stacked device of claim 81, wherein the stacked device is devoid of wire
2 bonds and TAB leads.

1 91. A method of making a three-dimensional stacked semiconductor package device,
2 comprising:

3 providing a first semiconductor package device that includes a first insulative housing, a
4 first semiconductor chip and a first lead, wherein the first insulative housing includes a first top
5 surface, a first bottom surface, and a first peripheral side surface between the first top and bottom
6 surfaces, the first chip is within the first insulative housing, the first chip includes a first upper
7 surface and a first lower surface, the first upper surface includes a first conductive pad, and the
8 first lead protrudes laterally from and extends through the first peripheral side surface, is
9 electrically connected to the first pad and is flat outside the first insulative housing;

10 providing a second semiconductor package device that includes a second insulative
11 housing, a second semiconductor chip and a second lead, wherein the second insulative housing
12 includes a second top surface, a second bottom surface, and a second peripheral side surface

13 between the second top and bottom surfaces, the second chip is within the second insulative
14 housing, the second chip includes a second upper surface and a second lower surface, the second
15 upper surface includes a second conductive pad, and the second lead protrudes laterally from and
16 extends through the second peripheral side surface, is electrically connected to the second pad
17 and is flat outside the second insulative housing;
18 bending the first lead downwardly outside the first insulative housing; then
19 positioning the first and second devices so that the second insulative housing overlaps the
20 first insulative housing, the second lead overlaps the first lead outside the insulative housings, the
21 top surfaces face upwardly, the bottom surfaces face downwardly, and the first top surface faces
22 towards the second bottom surface; and
23 electrically connecting the leads using a conductive bond that extends laterally beyond
24 any insulative material of the stacked device, extends downwardly beyond a surface of the first
25 chip and contacts the leads outside the insulative housings, wherein the first lead remains bent
26 and the second lead remains flat outside the insulative housings.

1 92. The method of claim 91, wherein the first upper surface faces towards the first
2 bottom surface, and the second upper surface faces towards the second bottom surface.

1 93. The method of claim 91, wherein the first lead extends downwardly beyond the
2 first bottom surface outside the first insulative housing, and the second lead does not extend
3 downwardly beyond the second bottom surface outside the second insulative housing.

1 94. The method of claim 91, wherein the first lead extends laterally from the first
2 peripheral side surface a first distance, the second lead extends laterally from the second
3 peripheral side surface a second distance, and the first distance is greater than the second
4 distance.

1 95. The method of claim 91, wherein the first lead outside the first insulative housing
2 includes inner and outer corners that are bent, an inner lateral portion that extends laterally
3 between the first peripheral side surface and the inner corner, a sloped portion that extends

4 laterally and downwardly between the inner and outer corners, and an outer lateral portion that
5 extends laterally between the outer corner and a distal end.

1 96. The method of claim 95, wherein the second lead outside the second insulative
2 housing is essentially identical to the inner lateral portion of the first lead.

1 97. The method of claim 91, wherein the conductive bond is spaced from the
2 insulative housings.

1 98. The method of claim 91, wherein the conductive bond is outside the peripheries of
2 the insulative housings.

1 99. The method of claim 91, wherein the conductive bond has a substantially
2 spherical shape.

1 100. The method of claim 91, wherein the stacked device is devoid of wire bonds and
2 TAB leads.